AMENDMENTS TO THE SPECIFICATION

After the Title, revise the first paragraph to read as follows:

This is a continuation of U.S. Patent application No. 10/121,790, filed April 10, 2002 and issued as U.S. Patent No. 6,864,500, and is related to U.S. patent application no. 10/618,824, filed July 14, 2003, now issued as U.S. Patent No. 6,838,307.

Amend the following paragraphs in the specification as shown:

[0005] In the case of a dielectric material, programmable capacitance between electrodes ~~are~~ is programmed by the extent of dendrite growth. In the case of resistive material, programmable resistances are also programmed in accordance with the extent of dendrite growth. The resistance of capacitance of the cell thus changes with changing dendrite length. By completely shorting the glass electrolyte, the metal dendrite can cause a radical change in current flow through the cell defining a different memory state.

[0032] Referring to FIG. 4, a spacer etch is performed, preferably by reactive ion etching (RIE), wherein horizontal portions 127 (FIG. 3) of the spacer layer 125 are removed, preferentially, leaving vertical portions of the spacer layer 125 relatively unaffected. FIG. 4 shows the vertical portions of the spacer layer 125 that remain after RIE< leaving a ~~the~~ spacer 131 lining vertical surfaces of the anode via 123. It will be understood that the spacer 131 forms a continuous lining around the sidewall of the anode via 123. In the illustrated embodiment, the spacer 131 is a cylindrical annulus with a rounded top edge, whose outer side surface is in contact with the sidewall of the abode via 123.

[0033] Next, as shown in Figure 5, a metal anode layer 133, preferably including a metal or combination of metals from Group IB or Group IIB, more preferably copper or zinc

and most preferably silver, is deposited. Preferably, the metal anode layer 133 is deposited so that it fills the anode via 123 and forms a portion 135 overlying the second insulating layer 121 all as one contiguous body of material. The ~~ovelying~~ overlying portion 135 is subsequently patterned and etched as desired, depending upon the circuit design of the memory array.

[0038] Thus, in one embodiment of the current invention, an anode via is made smaller than the cell body via so that the overlying insulator layer covers the cell body/insulator interface. The smaller anode vias are positioned so that their bottoms make contact only with the cell body and do not extend to the cell body/insulator interface. In another embodiment, a spacer prevents contact between the anode material and the cell body/insulator interface by covering the interface with spacer material near the outer edge of the anode via bottom. The preferred embodiments thus give reliable control to the spacing between the edge of the anode and the edge of the memory cell body or GFID material. These structures ensure that the anode cations that precipitate out to form the conductive path are those that were intentionally and controllably ~~provide~~ provided to the glass electrolyte material, whether by photodissolution, separate ~~metal-contining~~ metal-containing layer (see Figure 1~~c~~C), co-deposition or any other manner of metal doping. Silver content dissolved within a GeSe glass, for example, is self limiting at about 30 atm %, thus providing a reliably consistent source of diffusion ions for selectively forming the conductive path. For a given cation (e.g., Ag) concentration in solution, this provides conductive pathway formation reproducibly dependent upon voltage applied across the electrodes and/or switching time.